column. The eighth embodiment (FIG. 13) can therefore help not only to increase the [productivity] production of semiconductor integrated circuits, but also to reduce the manufacturing cost of semiconductor integrated circuits.

In the paragraph beginning at line 35 of column 9, enter the indicated amendment:

As shown in FIG. 14, a semiconductor memory to be tested has 24 pads arranged in eight rows and three columns. The probe card has group 19 of probe needles, each group consisting of 24 needles which are arranged in eight rows and three columns. FIG. 15 is a plan view showing how the probe needles of groups 19a to 19h are positioned with respect to the pads 31 of semiconductor memories 3a to 3h. (Shown in FIG. 15 are only groups 19a, 19b, 19g and 19h and only memories 3a, 3b, 3g and 3h.) As the probe card technology advances as expected, each group 19 may [consists] consist of more probe needles arranged in m rows and n column, where m>8 and n>3, whereby the probe card can test semiconductor integrated circuits each having more pads.

IN THE CLAIMS:

Please add new claims 6-16 as follows:

6. (New) A method of manufacturing semiconductor integrated circuit chips, comprising:

providing a semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged thereon in two columns and at least two rows, each of said plurality of semiconductor integrated circuit chips having a plurality of external terminals;

coupling a probe card to the semiconductor wafer through a plurality of probe needles on said probe card corresponding to said plurality of external terminals of each of said integrated circuit chips, said probe card receiving a plurality of independent test signals and a power supply signal from a tester;

concurrently supplying the independent test signals and the power supply signal from the tester through the probe needles to said plurality of external terminals of said plurality of integrated circuits; and

concurrently measuring electric characteristics of said semiconductor integrated circuit chips in an independent manner.

7. (New) The method of manufacturing of claim 6, wherein said external terminals are centrally disposed within said integrated circuit chips, with integrated circuits on either side of said external terminals.

8. (New) The method of manufacturing of claim 7, wherein said external terminals are arranged in a plurality of columns and rows.

9. (New) The method of manufacturing of claim 8, wherein said providing includes forming memory arrays for each of said integrated circuit chips.

10. (New) The method of manufacturing according to claim 6, wherein the test signal and the power supply signal are supplied from said tester to said probe needles by way of a plurality of wiring lines on internal layers of said probe card.

11. (New) The method of manufacturing according to claim 6, wherein the test signal and the power supply signal are supplied from said tester to said probe needles by way of a plurality of wiring lines on different internal layers of said probe card, said wiring lines positioned on different ones of said different internal layers according to a type of signal carried by said wiring lines.

12. (New) A probing test method of semiconductor integrated circuits, comprising:

preparing at least one semiconductor wafer, said semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged thereon in rows and columns, said semiconductor integrated circuit chips on each wafer arranged in two columns and at least two rows, each of said semiconductor integrated circuit chips having a plurality of external pads;

preparing at least one probe card, said probe card having a plurality of connection terminals for receiving from a tester a test signal and a power supply signal, said at least one probe card having a plurality of probe needles corresponding to said plurality of external pads, respectively;

supplying said test signal and said power supply signal from said tester to said probe needles by way of said connection terminals in a completely independent manner;

supplying said test signal and said power supply signal from said probe needles to said semiconductor integrated circuit chips, by way of said external pads, in a completely independent and concurrent manner; and

measuring electric characteristics of the semiconductor integrated circuit chips in a completely independent and concurrent manner.

13. (New) The probing test method according to claim 12, wherein said test signal and said power supply signal are supplied from said connection terminals to said probe needles in a completely independent and concurrent manner, by way of a plurality of completely independent wiring lines which are provided inside said probe card and to which said test signal and said power supply terminal are transmitted.

14. (New) The probing test method according to claim 12, wherein said test signal and said power supply terminal are supplied from said connection terminals to said probe needles in a completely independent and concurrent manner, by way of a plurality of wiring lines which are provided inside said probe card in accordance with kinds of signals and types of power supplies.

15. (New) The probing test method according to claim 12, further comprising:
preparing at least one test station; and
attaching said probe card to said at least one test station.

16. (New) The probing method according to claim 12, further comprising:
preparing at least one test station; and
attaching a plurality of probe cards to said at least one test station.